REMARKS

Applicants wish to thank the Examiner for the courteous and helpful telephone interview granted Applicants' representative on February 23, 2006. The present Amendment has been prepared pursuant to comments and suggestions made by the Examiner during the interview.

Claims 1-27 are pending in the present application. Claims 1-4, 6, 7, 10-13, 15, 16, 19-22 , 24 and 25 were amended. No claims have been added and no claims have been canceled. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims currently in the case patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

The specification has been amended to supply the missing information concerning related applications referred to therein. No new matter has been added by any of the amendments to the specification.

I. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 7, 10, 16, 19 and 25 under 35 U.S.C. § 102(b) as being anticipated by Mason et al. (U.S. Patent No. 5,926,640). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> As per claim 1, the reference of Mason et al. teaches, "an interrupt unit; wherein the interrupt unit receives a signal for initiating an interrupt" in Fig. 1, elements 50 and 66; "wherein the interrupt unit counts the occurrence of interrupts by type" in abstract, lines 9-11 and col. 3, lines 58-60.

Office Action dated December 2, 2005, page 2.

Claim 1 of the present application as amended herein is as follows:

> 1. A data processing system, comprising:
> an interrupt unit for receiving a signal for initiating an interrupt, the interrupt unit comprising a plurality of counters for counting the occurrence of a plurality of different types of interrupts by interrupt type; and
> a storage for storing a count value of each of the plurality of interrupt types.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Mason et al. (hereinafter "Mason") does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to amended claim 1, in particular, Mason does not teach or suggest an interrupt unit that comprises "a plurality of counters for counting the occurrence of a plurality of different types of interrupts by interrupt type; and "a storage for storing a count value of each of the plurality of interrupt types".

Mason is directed to a method for reducing power consumption in a computer system. Mason discloses that "interval clock interrupts" occur at periodic intervals in a data processing system, and typically requires a CPU to repeatedly awaken from a low power consumption state to service the interrupts. The invention in Mason provides a mechanism that counts assertions of an interval interrupt signal, and returns the CPU to a normal power consumption mode when either a predetermined time period has expired or a system interrupt signal other than an interval interrupt signal is asserted (see col. 2, lines 18-27 of Mason). In this way, the CPU can remain in a low power consumption state for longer periods of time thus conserving energy.

Mason may provide a mechanism for counting interval interrupt signals. Mason does not, however, disclose "a plurality of counters for counting the occurrence of a plurality of different types of interrupts by interrupt type", and does not disclose "a storage for storing a count value of each of the plurality of interrupt types" as now recited in claim 1. As pointed out in the present specification, the present invention enables interrupts, such as, for example, a TLB (translation lookaside buffer) fault and a VHPT (virtual hash page table) Instruction fault to be counted by type; and the gathered information may be used to assist in analyzing data processing system performance.

Inasmuch as Mason does not disclose or suggest "a plurality of counters for counting the occurrence of a plurality of different types of interrupts by interrupt type" as now recited in claim 1, and also does not disclose or suggest "a storage for storing a count value of each of the

plurality of interrupt types" as further recited in claim 1, claim 1 is not anticipated by Mason and should be allowable over Mason in its present form.

Claim 7 depends from and further restricts claim 1, and is also not anticipated by Mason, at least by virtue of its dependency.

Independent claims 10 and 19 have been amended in a manner generally similar to claim 1, and are also not anticipated by Mason for similar reasons as discussed above with respect to claim 1. These claims, therefore, should also be allowable in their present form, and it is respectfully requested that the Examiner so find.

Claims 16 and 25 depend from and further restrict claims 10 and 19, respectively, and are also not anticipated by Mason, at least by virtue of their dependency.

Therefore, the rejection of claims 1, 7, 10, 16, 19 and 25 under 35 U.S.C. § 102 has been overcome.

Furthermore, Mason does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Mason teaches a method for monitoring an interval interrupt signal to reduce power consumption in a computer system, and is not related to a plurality of counters for counting the occurrence of a plurality of different types of interrupts by interrupt type as presently recited in claim 1. Absent the Examiner pointing out some teaching or incentive in Mason, one of ordinary skill in the art would not be led to modify Mason to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Mason in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' own disclosure as a template to make the necessary changes to reach the claimed invention.

II. 35 U.S.C. § 103, Obviousness – Claims 2, 3, 11, 12, 20 and 21

The Examiner has rejected claims 2, 3, 11, 12, 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Mason et al. (U.S. Patent No. 5,926,640) in view of Shek et al. (U.S. Patent No. 6,185,652 B1). This rejection is respectfully traversed.

With respect to claim 3, the Examiner cites Shek et al. (hereinafter "Shek") as disclosing "wherein a count of an interrupt type is stored in an entry of an interrupt count table", and refers to col. 9, lines 48-50 of Shek. Col 9, lines 45-53 is as follows:

> The address table **156** is an ordered list of all of the tasks **85** sent by the CPU **108** to the NorthBay **112** for execution since some past event known to the CPU **108**. From this table **156**, given an interrupt count **152** or an interrupt address **154**, the CPU **108** can determine the tasks **85** that have been executed by the NorthBay **112** and therefore how many tasks **85** and/or scripts

109 remain to be executed by the NorthBay 112. When the NorthBay 112 is in need of more data to process the script composer 146 generates additional scripts 109 reflecting the queued host requests 162. One embodiment of the address table 156 is described below with reference to FIG. 6.

Claim 3 as amended herein is as follows:

3. The data processing system of claim 1, wherein the storage comprises an interrupt count table outside of an interrupt descriptor table of the system, the interrupt count table storing a count value of an interrupt type in an entry of the interrupt count table.

Shek does not supply the deficiencies in Mason as described above, and claim 3 should be allowable over the references, at least by virtue of its dependency from claim 1, In addition, the address table in Shek is an ordered list of tasks sent by the CPU to the Northbay for execution. Shek does not disclose that this table comprises an "interrupt count table outside of an interrupt descriptor table of the system" or that the table stores a "count value of an interrupt type in an entry of the interrupt count table" as recited in claim 3. Claim 3, accordingly, should be allowable over Mason in view of Shek in its own right as well as by virtue of its dependency.

Claims 12 and 21 have been amended in a manner similar to claim 3, and should also be allowable in their present form, both in their own right and by virtue of their dependency from allowable claims.

With respect to claims 2, 11 and 20, the Examiner asserts that these claims are rejected for similar reasons as claims 3, 12 and 21 because they do not claim any patentable distinguishing feature. By the present Amendment, these claims have been clarified to recite that the interrupt descriptor table "associates each interrupt with a corresponding interrupt handler". Neithr Mason nor Shek discloses or suggests "wherein the storage comprises an interrupt descriptor table that associates each interrupt with a corresponding interrupt handler, the interrupt descriptor table storing a count value of an interrupt type in an entry of the interrupt descriptor table" as now recited in claim 2, and claim 2 should be allowable in its own right as well as by virtue of its dependency from claim 1.

Claims 11 and 20 have been amended in a manner similar to claim 2, and should also be allowable in their present form.

Therefore, the rejection of claims 2, 3, 11, 12, 20 and 21 under 35 U.S.C. § 103 has been overcome.

III. 35 U.S.C. § 103, Obviousness – Claims 9, 18 and 27

The Examiner has rejected claims 9, 18 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Mason et al. (U.S. Patent No. 5,926,640) in view of Soga (U.S. Patent No.4,145,735). This rejection is respectfully traversed.

Soga is cited as disclosing "wherein when a count is about to overflow, an overflow signal is sent". Soga, however, does not supply the deficiencies in independent claims 1, 10 and 19 as discussed above, and claims 9, 18 and 27 should be allowable in their present form at least by virtue of their dependency from allowed claims.

Therefore, the rejection of claims 9, 18 and 27 under 35 U.S.C. § 103 has been overcome.

IV. Objection to Claims

The Examiner has stated that claims 4-6, 8, 13-15, 17, 22-24 and 26 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the Examiner's indication of the allowability of those claims. In response, claims 4, 6, 13, 15, 22 and 24 have been rewritten in independent form including all of the limitations of their base claim and any intervening claims, and should now be allowed, together with claims 5, 14 and 23 which depend from claims 4, 13 and 22, respectively. Claims 8, 17 and 26 remain as dependent claims, and should continue to be allowable in their present form.

V. Conclusion

For all the above reasons, it is respectfully urged that claims 1-27 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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